DELTA TAU
EUROPA

7th generation

POWER PMAC

Multiple axis machine computer

The new Power PMAC from Delta Tau is a seventh generation motion controller that combines unprecedented speed and accuracy with ultra high bandwidth for sub-nanoscale motion precision.

Control up to 256 axes from a single card with a unique 64-bit hardware floating point processor that delivers breathtaking processing speeds – that's orders of magnitude better than other motion controllers. In one customer servo program test processing time was slashed from 588µs to just 1.6 µs. There is also the capability to control up to 32 co-ordinated axes.

High speed integrated communications aids precision machine implementation and control. Again, a custom test showed an improvement from 4.0s to 220ms.

New memory configurations enable extremely fast access rates and the Power PMAC boasts not only error checking, but importantly now has error correction – a vital new feature for improved system reliability.

Other standard features include powerful PLC functionality; a web server interface as standard; USB and SD card interfaces; and USB2 built in Ethernet with 1GB transmission. The Integrated Development Environment (IDE) for Power PMAC integrates seamlessly into MS Visual Studio.

Look at these features

Control up to 256 axes

Control up to 32 co-ordinated axes

32/64-bit architecture

64-bit hardware floating point implementation

Compiled PLCs can be written in C

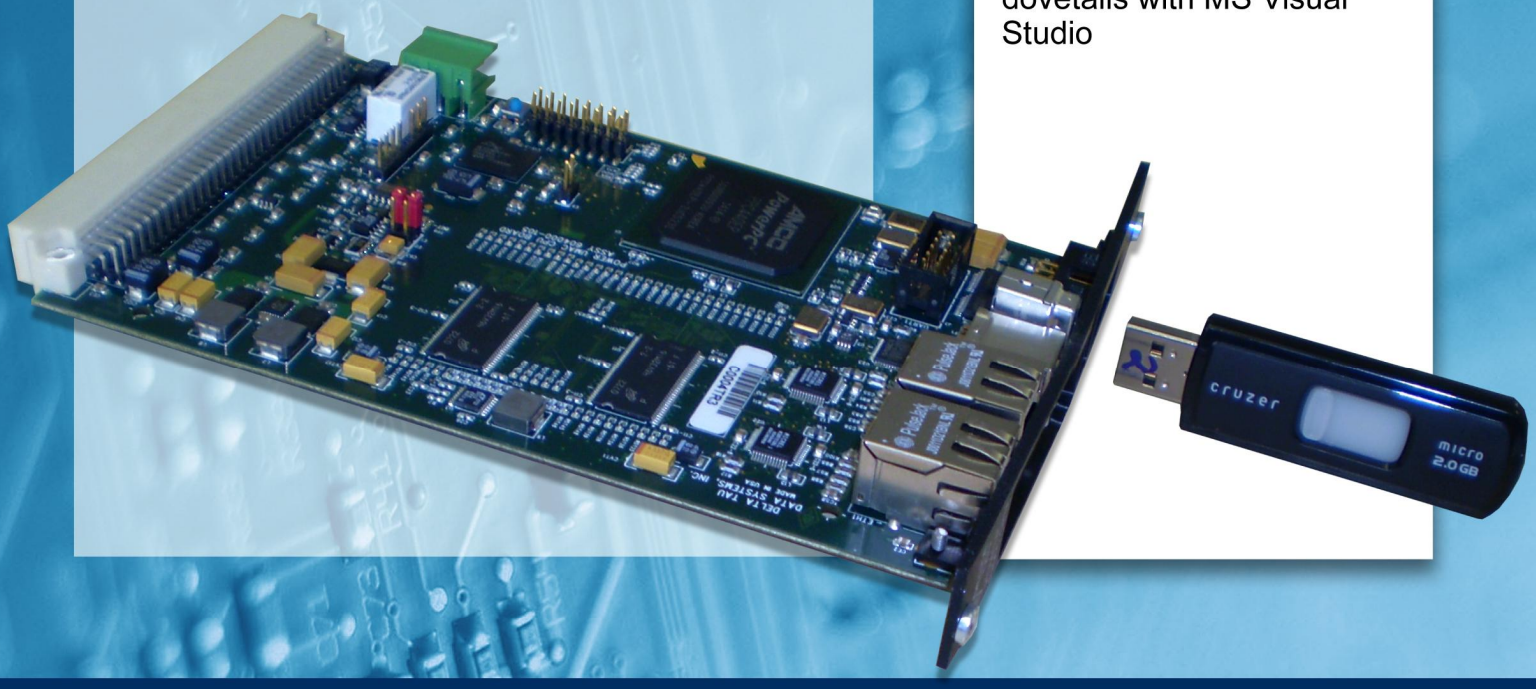
USB2 1GB Ethernet capability

USB and SD card interfaces

Plus!

Web server interface

Software Integrated Development Environment (IDE) dovetails with MS Visual Studio



The next generation motion computer

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Introduction

Delta Tau's 7th generation controller family, called "Power PMAC", uses advanced processor architecture, ASIC capabilities, software tools, and sophisticated algorithms to advance motion and machine control.

Addressing Space

The processor has full 32-bit data and address buses, giving it the capability to support large amounts of memory and I/O. It interfaces directly to large but inexpensive PC RAM ICs (DDR SDRAM), providing over an order of magnitude more memory. Very large programs are stored in the controller's memory, eliminating the need to stream in real time. For high-reliability operation there is error-correction code RAM.

Floating-Point Maths

The processor's integrated hardware implementation of 64-bit floating-point maths processing provides far greater speed than previously possible, with an extended dynamic range as well. The processor integrates many DSP-type features as well, further speeding calculations. Hardware floating-point processing yields computations five times faster than present capabilities.

Compiler Support

Software development is faster and easier to debug. Both proprietary and open-source (e.g. GNU) compilers are available In addition, the code can easily be compiled for other processors, such as Intel's Pentium class (and compatible) processors.

Built-In Peripherals

The new embedded processors have many peripheral functions built in, which will make the controllers more compact and cost effective. Built-in interfaces include USB2.0, 100Mbps Ethernet, and PCI bus.

ASIC

The new ASIC (the PMAC3 ASIC) provides powerful capabilities when used with the Power PMAC processors.

Software

Power PMAC's greater speed, numerical range, addressing range, and ease of programming will permit powerful new software capabilities in many aspects. Delta Tau has made programing simpler, for example: software is powered by VS 2005; it's a full featured Windows-based system; has limited featured web-based system; offers a familiar environment for those who already program; an easy to use for non-programmers. There are also

New algorithms that the increased capabilities permit range from

New algorithms that the increased capabilities permit range from very sophisticated (e.g. jerk imitation in lookahead) to basic imitation in lookahead) to basic capabilities that have been too time-consuming before (e.g. multiple types of checks for invalid motion commands).

User Programming Styles

The new controller supports user programming both in the PMAC style, with a language that is similar to G-Codes and BASIC, and does not require upper-level software expertise. In this style, the programs are executed by the controller's built-in scheduler/interpreter, so the user does not face the most difficult task of allotting processor time and priority.

NC Features

Limitation of jerk (as well as acceleration, velocity, and position) is enabled in lookahead algorithms, providing smooth S-curve acceleration on arbitrary trajectories, including sharp corners. The lookahead algorithm can store programmed block-end as well as intermediate segment positions, permitting both accurate "distance-to-go" reporting, and the ability to stop at block-end positions (respecting acceleration limits) even if the lookahead has gone beyond this particular block.

Configurations

Power PMAC is available in multiple configurations, including UMAC rack-mounted system and PC-based expansion cards, both with built-in machine interfaces, and with MACRO for remote machine interfaces.

System capabilities

Specification	Turbo PMAC	Power PMAC
CPU Frequency	<= 240 MHz	>=400 MHz
External Data Bus Width	24 bit	32 bit
Internal Data Bus Width	48 bit	64 bit
Address Bus Width	19 bit	32 bit
Maximum Memory Capacity	1M x 24	64M x 32
Memory Type	SRAM	DDR SDRAM
Non-Volatile Configuration Storage	Flash memory	Flash memory
Quick Non-Volatile Parameter Storage	Battery-backed RAM	Battery-backed RAM
Floating-Point Implementation	Software	Hardware
Floating-Point Length	48 bit	64 bit
Floating-Point Relative Speed	1	5
Phase Commutation Math Type	Fixed-Point	Floating-Point
Servo/Interpolation Math Type	Fixed-Point	Floating-Point
C Compiler Support	Poor	Excellent
Firmware Implementation	Assembly language	C, C++
User Programming Implementation	G-Code/Basic	G-Code/Basic, C, C++
Number of Motors	32	256
Number of Coordinate Systems	16	32+
Number of I-Variables	8192	16384+
Number of P-Variables	8192	16384+
Number of Q-Variables	8192	16384+
Number of M-Variables	8192	16384+
Number of L-Variables	8192	16384+
Variable Macro Substitution	In PC	In controller
Parameters Limited by Lookahead	Position, velocity, acceleration	Position, velocity, acceleration, jerk
PCI Implementation	FPGA	Built-in
USB 2.0 Implementation	Microcontroller	Built-in (x2)
100 Mbps Ethernet Implementation	Microcontroller	Built-in (x2)
Serial Port Implementation	1 built-in, 1 external	4 built-in
Data Streaming Method	Dual-ported RAM	DMA
MACRO Raw Bit Rate	125 Mbps	1.25 Gbps
MACRO Data Packet Size	9 bytes (1x3, 3x2)	16 bytes (4x4)
MACRO Byte Data Check	2x 4B/5B	8B/10B
MACRO Packet Data Check	Longitudinal Parity	CRC

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Delta Tau Europa AG, Gewerbestrasse 8, 8212 Neuhausen, Switzerland. Tel: +41 52 62 52 088
www.deltatau.com